> a silicon substrate having a first and second surface; a first layer disposed on said first surface and having impurities of the N or P conductivity type uniformly distributed throughout the volume of said first layer; a second layer disposed on said first layer said second layer having impurities of the same type as those in said first layer uniformly distributed therethrough; the concentration of impurities in said second layer being greater than the concentration of impurities in said first layer; said first layer and said second layer having generally coincident boundaries.

Muramoto does not teach or suggest the present invention's use of a first and second layer having generally coincident boundaries. As is clearly seen from the figures, even if the Muramoto layer 12 is considered to be the second layer, it does not have generally coincident boundaries with the first layer and does not reduce the resistance contribution from both the JFET region and the bottom epitaxial layer as does the present invention. Only by using a first and second layer with generally coincident boundaries and having a different impurity gradient between them can the advantages of the present invention be realized.

Also, the second layer of the present invention has a higher doping concentration than the traditional device (such as shown in Muramoto) so that the lateral P^+ diffusion in the JFET region is smaller and the resistivity of the epitaxial layer is reduced. Both of these effects give rise to the present invention's 10% reduction in the on resistance over the prior art. The Muramoto reference discloses nothing more than Figure 1 of the instant application and does not disclose or suggest the present invention's novel two layer device where the first layer has a higher resistivity than that of the second layer and where the first layer is also thicker than the second layer. The net effect of this combination is to reduce the on resistance of the device by more than over 10% over the prior art as well as providing a device that is thinner in its overall dimensions.

Likewise, independent claim 10 also recites

> A device where the layer and the upper surface have generally coincident boundaries. The layer has a graded concentration of the conductivity types where the upper portion has a lower resistivity than the lower portion yet the lower portion comprises more than 50% of the total thickness of the layer.

For the reasons discussed above, independent claim 10 should be patentable over the art of record.

Many semiconductor devices are layered in nature, however, specific combinations lead to very different results. The present application's use of layers to achieve the result of reducing the on-resistance by over 10% is proposed to be patentable over the prior art.

Dependent claims 2-8 and 11-12 are dependent either directly or indirectly from either claim 1 or claim 10. It is respectfully submitted that dependent claims 2-8 and 11-12 are patentable for the same reasons advanced above in connection with claims 1 and 10 as well as because of the combination of the features set forth in these claims with the features set forth in the claim(s) from which they depend.

Claims 1, 2 and 9 are rejected under 35 U.S.C. §102(b) as being anticipated by Merrill. Applicants respectfully traverse this rejection.

The Examiner states that Merrill discloses the present invention and refers to Figures 4 and 20 comprising a silicon substrate 51 of first epitaxial silicon layer 52 and a second epitaxial silicon layer 180. Applicants respectfully submit that Merrill actually teaches away from the present invention. In order to anticipate a reference must recite all of the elements and have them in the same order as the invention. Merrill teaches exactly the opposite configuration from the present invention. The Merrill device uses a first layer with a lower resistivity and thinner than the second layer. While the Merrill device does reduce the on-resistance, it does not reduce it to the same degree nor is it as easily made as the present invention. A person skilled in the art following Merrill, while being led to adjust the thicknesses and resistivities of the regions, would have no reason to completely invert them making the first layer thicker with a higher resistivity than the thin lower resistivity second layer.

Amended claim 1 comprises, inter alia, a first layer disposed on said first surface and having impurities of the N or P conductivity type uniformly distributed throughout the volume of the first layer. A second layer disposed on said first layer said second layer having impurities of the same type as those in said first layer uniformly distributed therethrough the concentration of the impurities in the second layer being greater than the concentration of the impurities in said first layer. Dependent claim 2 further clarifies that the second layer has a lower resistivity than the first layer exactly opposite the teaching of Merrill. Likewise,

independent claim 10 has a lower resistivity in the upper portion of the layer. Applicants respectfully propose that since Merrill teaches away from the present invention's lower resistivity thinner upper layer, claims 1, 2 and 9 are patentable over Merrill.

Claims 3-8 and 10-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Merrill. Applicants respectfully traverse this rejection.

The Examiner asserts that routine experimentation and optimization makes the present invention obvious over Merrill. Nothing in Merrill teaches or suggests that the thickness and resistivity should be completely reversed. While experimentation could vary the relative values (as pointed out in the Merrill disclosure), Applicants respectfully submit that it is too far a stretch to say that a complete reversal would be routine experimentation. Merrill discloses a device with a thinner first layer with a lower resistivity than the thick second layer with a higher resistivity exactly opposite the present invention.

For the reasons advanced above, applicants propose that independent claim 10, as amended, requires a first layer with increased resistivity and thicker than the second layer with a lower resistivity in exact contradiction to the Merrill reference. There is no suggestion or teaching to reverse the Merrill device. Certainly the motivation did not exist in the general knowledge in the art, nor was it well known since it had not been done before. Applicants respectfully propose that independent claim 10, as amended, is patentable over Merrill.

Dependent claims 3-8 and 11-12 are dependent either directly or indirectly from either claim 1 or claim 10 and are therefore patentable for the same reasons advanced above in connection with claims 1 and 10 as well as because of the combination of the features set forth in these claims with the features set forth in the claim(s) from which they depend.

Claims 1-12 are further rejected under 35 U.S.C. §102(b) as anticipated by, or in the alternative, under 35 U.S.C. §103(a) as obvious over Hshieh. Applicants respectfully traverse this rejection.

Independent claim 1, as amended, is directed towards a semiconductor device comprising, inter alia, a first layer disposed on said first surface having impurities of the N or P conductivity type uniformly distributed throughout the volume of said first layer a second layer disposed on said first layer said second layer having impurities of the same type as those in said first layer uniformly distributed therethrough. The concentration of impurities in said second

layer being greater than the concentration of impurities in said first layer said first surface, said first layer and said second layer having generally coincident boundaries. Referring to Figures 2 and 3 of the Hshieh reference, it is easily seen that the first and second layers cannot have coincident boundaries. A trench lined with an oxide 24 passes completely through the second layer but only partially through the first layer, therefore, the two layers cannot have coincident boundaries. Hshieh is trying to reduce the lateral diffusion of the P^+ body so that the cell density of the trench DMOS can be increased. It is completely silent about the on-resistance of each cell. The present invention's use of layers having generally coincident boundaries reduces the on-resistance by more than 10% over the conventional devices.

Since it is shown that the Hshieh reference does not disclose the two layers having generally coincident boundaries, Applicants respectfully propose that independent claim 1, as amended, is patentable over the Hshieh reference.

Likewise, independent claim 10, as amended, recites a layer and an upper surface having generally coincident boundaries and therefore, should be patentable over the Hshieh reference for the same reasons as advanced above.

Dependent claims 2-9 and 11-12 are dependent either directly or indirectly from either claim 1 or claim 10 and are therefore patentable for the same reasons advanced above in connection with claims 1 and 10 as well as because of the combination of the features set forth in these claims with the features set forth in the claim(s) from which they depend.

In view of the foregoing, this application is now believed to be in condition for allowance which action is respectfully requested.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231, on November 3, 2000:

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Name of applicant, assignee or Registered Representative

Signature

November 3, 2000
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Respectfully submitted,

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